

## BEE 233 Circuits

Fall 2015

### Lab 4: Opamp filters instructor's notes

#### 4 Circuits

These are the five opamp circuits in this lab. In all cases, the opamp is the same LM348 you worked with in Lab 3,  $V_{CC} = +12\text{ V}$  and  $V_{EE} = -12\text{ V}$ .

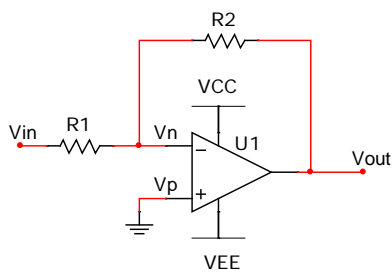


Figure 1. Inverting amplifier.

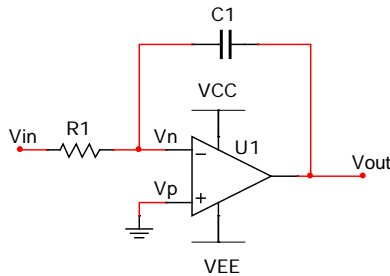


Figure 2. Simple integrator.

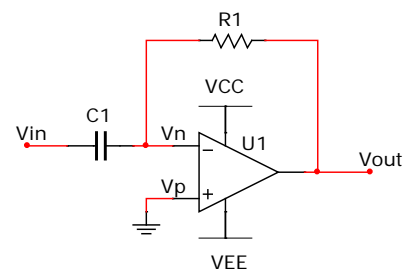


Figure 3. Simple differentiator.

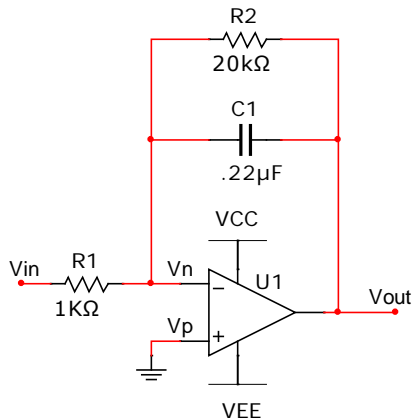


Figure 4. Integrator with shunt.

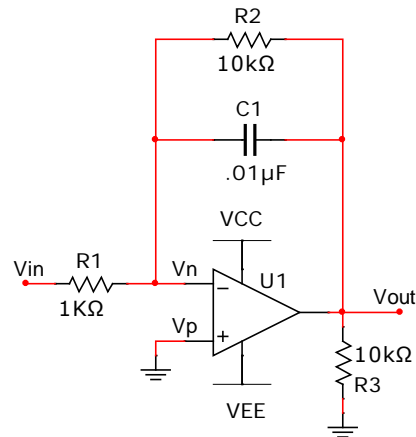


Figure 5. Low-pass filter.

## 5 Inverting amplifier

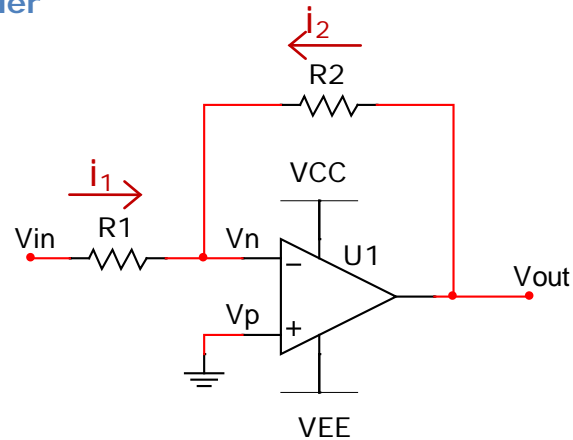


Figure 12. Inverting amplifier.

1. Analyze the inverting amplifier circuit in figure 12 (same as figure 1) to derive an equation for the gain,  $A_v$ , as a function of  $R_1$  and  $R_2$ .

$$V_n = V_p = 0$$

$$i_1 = -i_2$$

$$V_{in} = i_1 R_1 + V_n = i_1 R_1$$

$$V_{out} = i_2 R_2 + V_n = i_2 R_2 = -i_1 R_2$$

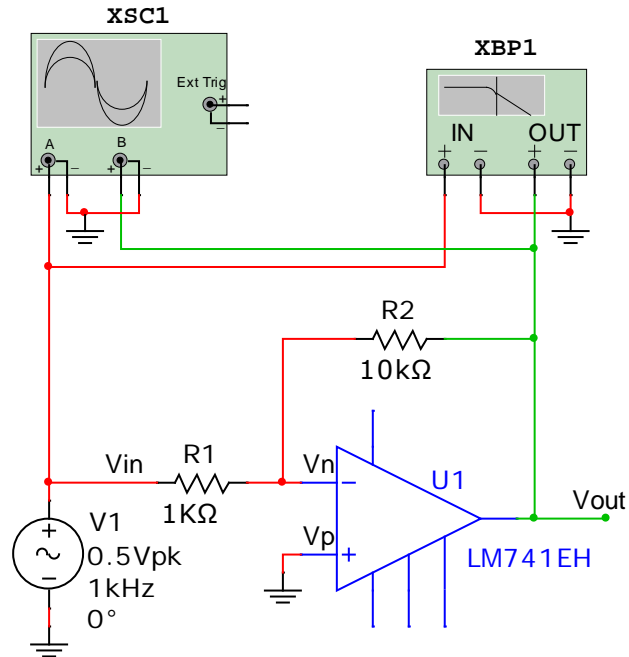
$$A_v = \frac{V_{out}}{V_{in}} = -\frac{i_1 R_2}{i_1 R_1} = -\frac{R_2}{R_1}$$

2. Choose values for  $R_1$  and  $R_2$  to produce a gain,  $A_v = -10$ .

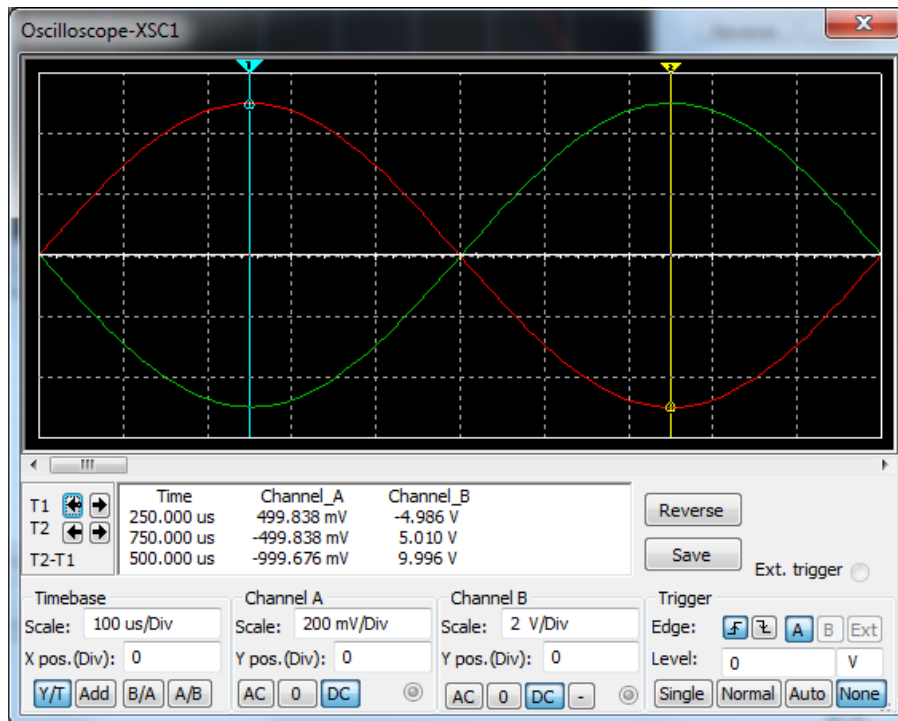
For  $A_v = -10$  and  $R_1 = 1 \text{ K}\Omega$ ,  $R_2 = 10 \text{ K}\Omega$

3. Simulate your circuit. Capture images of the following.
  - a. Your schematic.

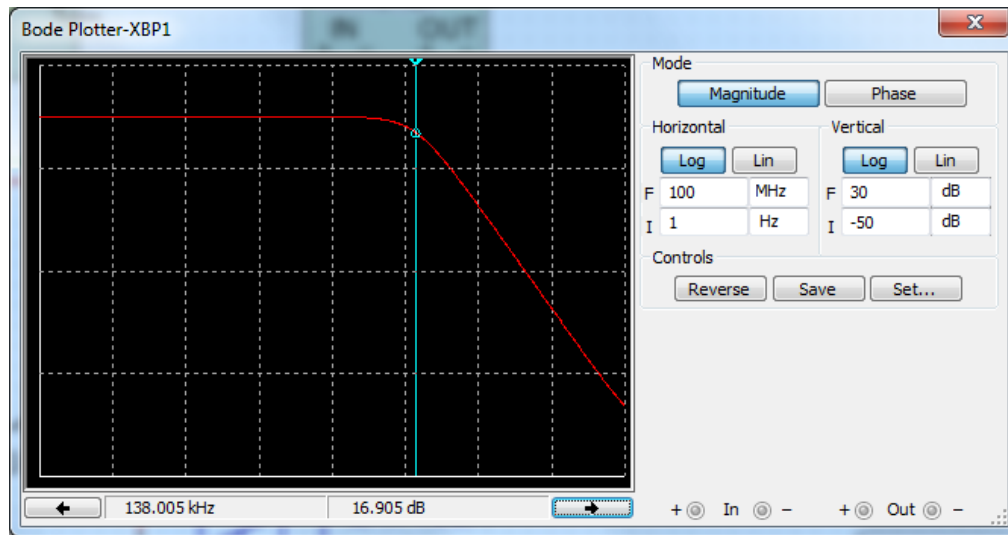
You should have built something like this and gotten results similar to the following.



- b. An oscilloscope display of  $V_{in}$  and  $V_{out}$  for  $V_{in} = 1.0$  Vpp, 1 KHz sine wave, 0 V DC offset.



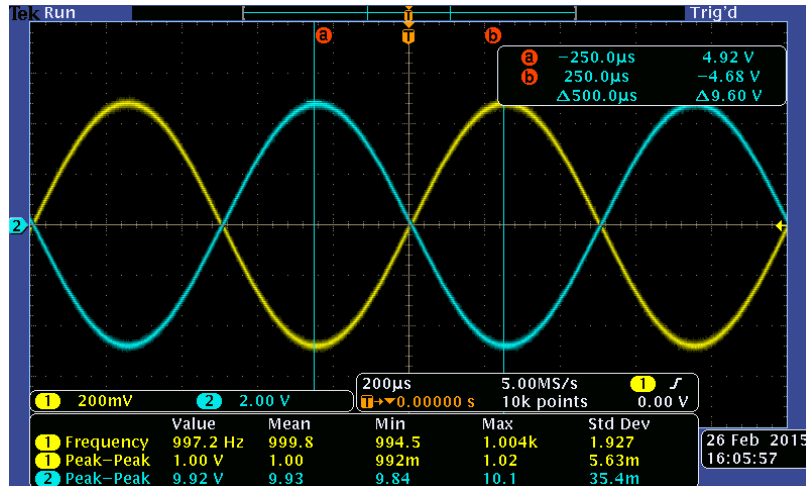
- c. A Bode plot of the frequency response with a cursor at the cutoff frequency.

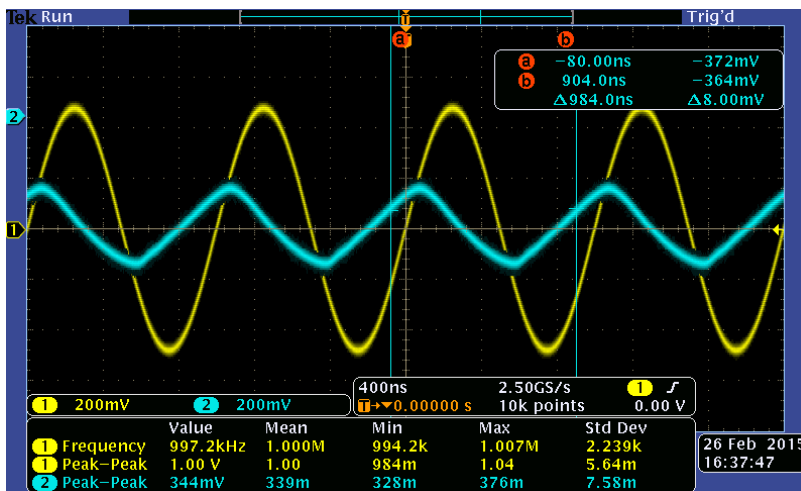
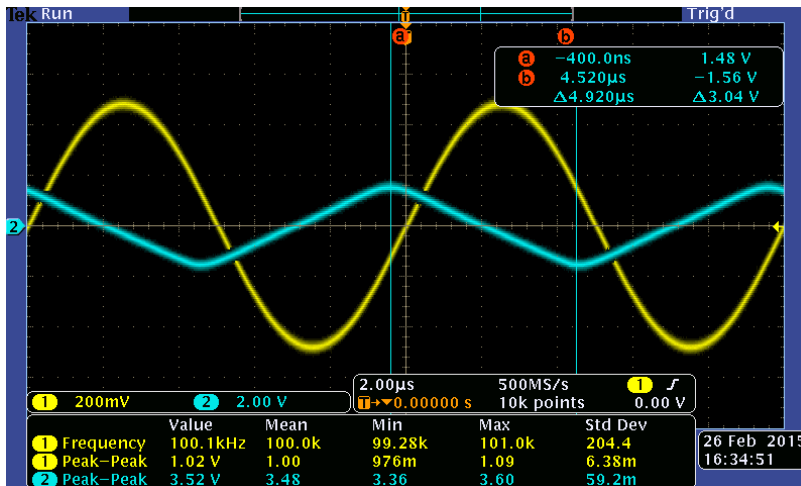


Cutoff was at about 138 KHz in the model that came with my copy of Multisim.

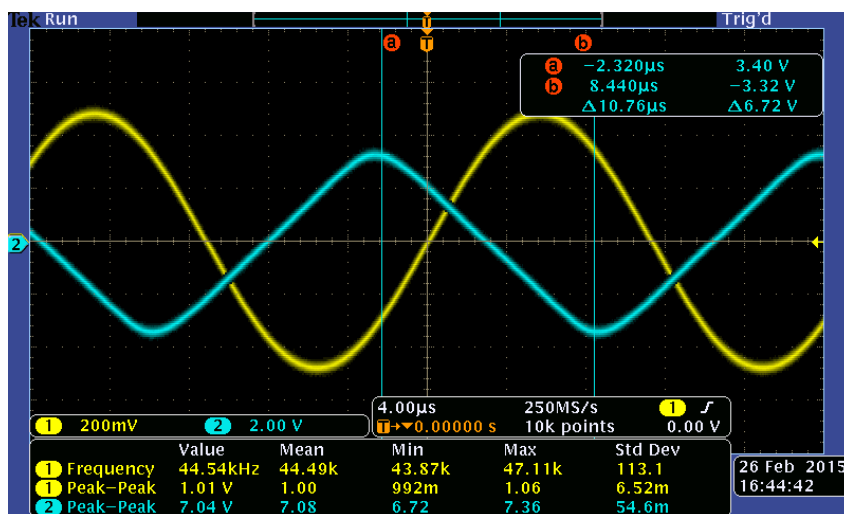
4. Breadboard the circuit and capture screenshots with  $V_{in} = 1.0$  Vpp sine wave, 0 V DC offset, at 1 KHz, 100 KHz and 1 MHz.

You probably got results about like this. I should have asked for a smaller value of  $V_{in}$  to reduce the effect of hitting slew rate limits.





5. Find the cutoff frequency at which gain has dropped by 3 dB and capture a screenshot.



6. Create a table of measurements at increasing frequencies from 100 Hz to 1 MHz in a 1-2-5-10 sequence. Try to hold  $V_{in}$  fairly constant as you increase the frequency.

Frequency (Hz)	$V_{in}$	$V_{out}$	Gain ( $A_v$ )	Gain (dB)
100	Your data goes here			
200				
500				
1K				
2K				
:				
500K				
1M				

7. Create a Bode plot of Gain(dB) versus frequency from your measurements.

Your plot goes here.

8. Compare the Bode plots and cutoff frequencies based on your simulation with your experimental results and explain any differences.

Your actual cutoff was probably a lot lower than predicted by simulation, perhaps because the model was wrong or doesn't quite match your chip or because it calculated the Bode plot using smaller input signals than we used and avoided slew rate limits. It's also possible your breadboard added additional stray capacitance or inductance not accounted for in the model.

## 6 Simple integrator

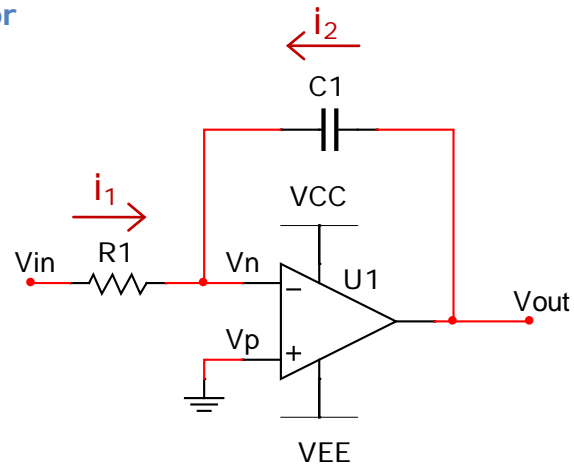


Figure 13. Simple integrator.

1. Analyze the integrator circuit in figure 13 (same as figure 2) to derive an equation for  $V_{out}(t)$  as a function of  $V_{in}(t)$ . Show that the output is the integral of the input.

$$V_{in} = i_1 R_1$$

$$i_1 = \frac{V_{in}}{R_1} = -i_2$$

$$V_{out} = \int_0^t \frac{i_2}{C_1} dt$$

$$V_{out} = - \int_0^t \frac{V_{in}}{R_1 C_1} dt = - \frac{1}{R_1 C_1} \int_0^t V_{in} dt$$

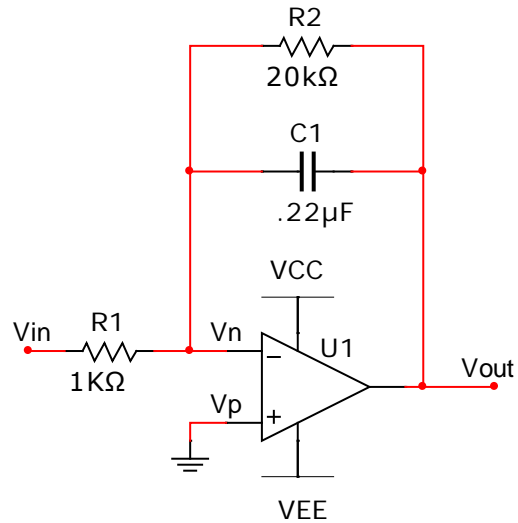


Figure 14. Integrator with shunt.

2. Analyze the circuit in figure 14 (same as figure 4) to calculate the low-frequency gain. Show that for  $\gg \frac{1}{R_2 C_1}$ , this circuit also functions as integrator.

All that's required here is a hand-waving argument about what happens at low frequencies, where we can ignore the capacitor, and at high frequencies, where we can ignore the resistor.

At low frequency,  $Z_{C1} \rightarrow \infty$ , making it behave like the inverting amp in 6.1.

$$A_v = -\frac{R_2}{R_1} = -\frac{20 \text{ K}\Omega}{1 \text{ K}\Omega} = -20$$

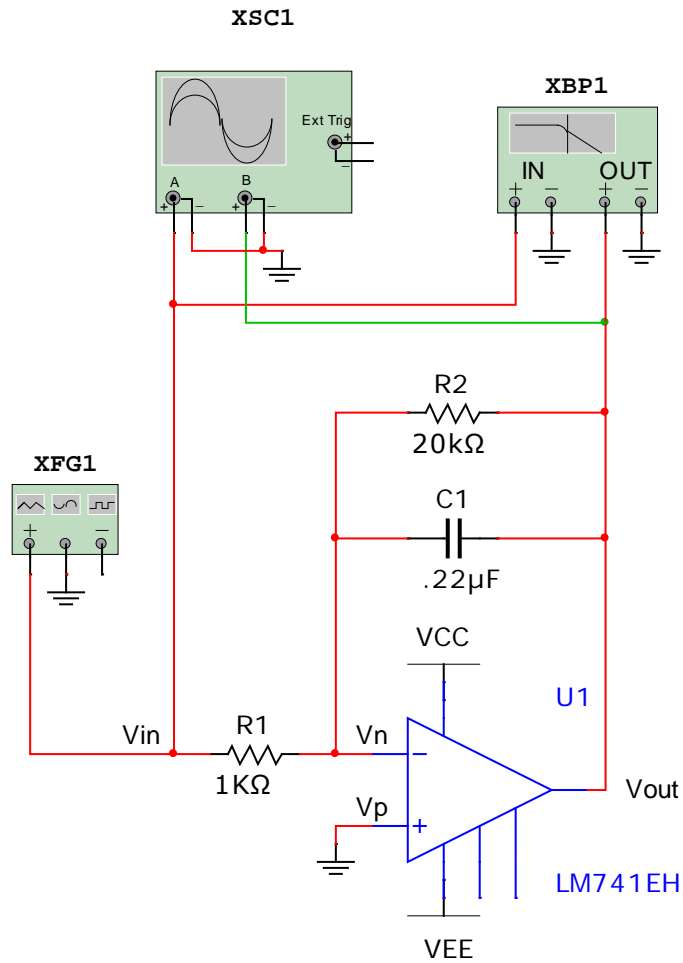
At high frequency, the impedance of the capacitor is much less than that of  $R_2$ , making it behave like an integrator.

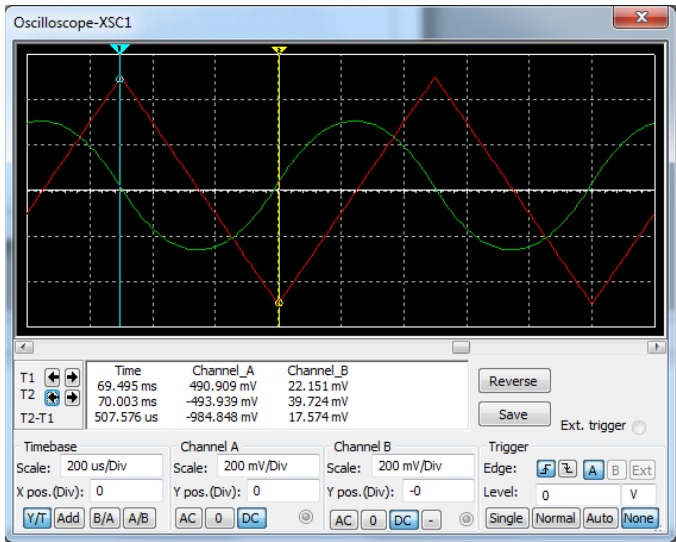
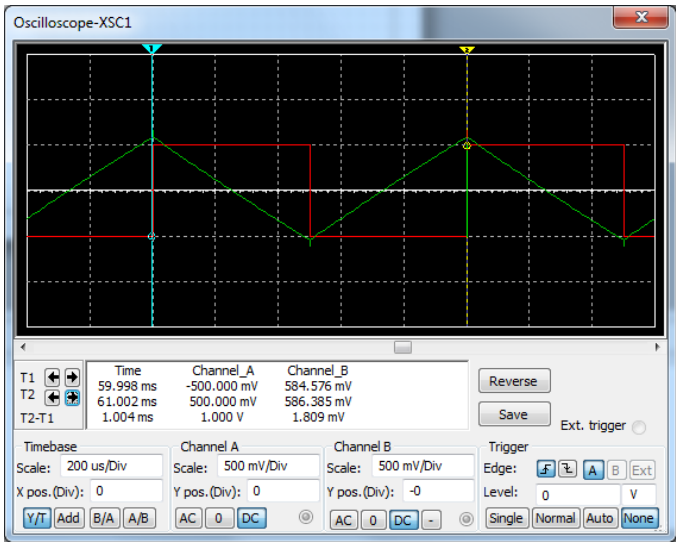
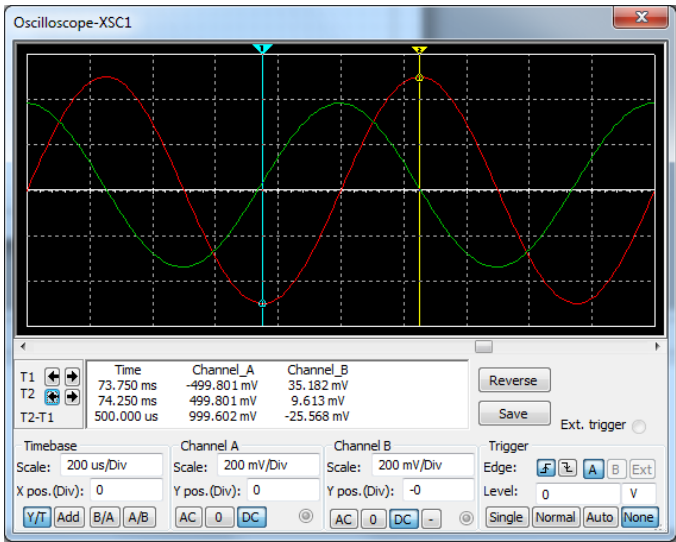
$$Z_{C1} = \frac{1}{sC_1} \ll R_2$$



3. Simulate this circuit and capture images of your schematic and of oscilloscope displays of  $V_{in}$  and  $V_{out}$  with  $V_{in}$  set to be a sine wave, a square wave and a triangle wave. In each case, set  $V_{in} = 1.0$  Vpp at 1 KHz, 0 V DC offset.

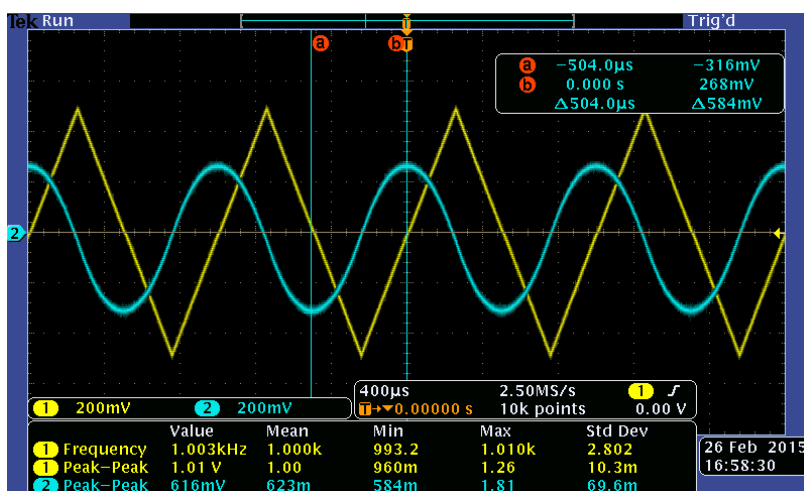
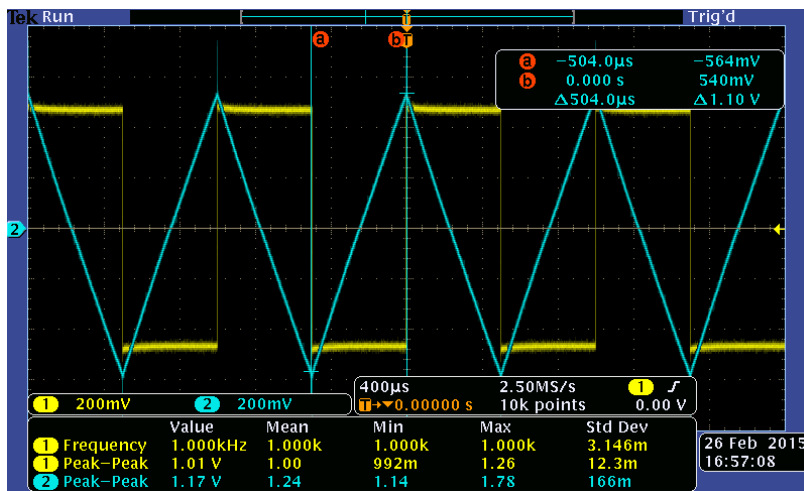
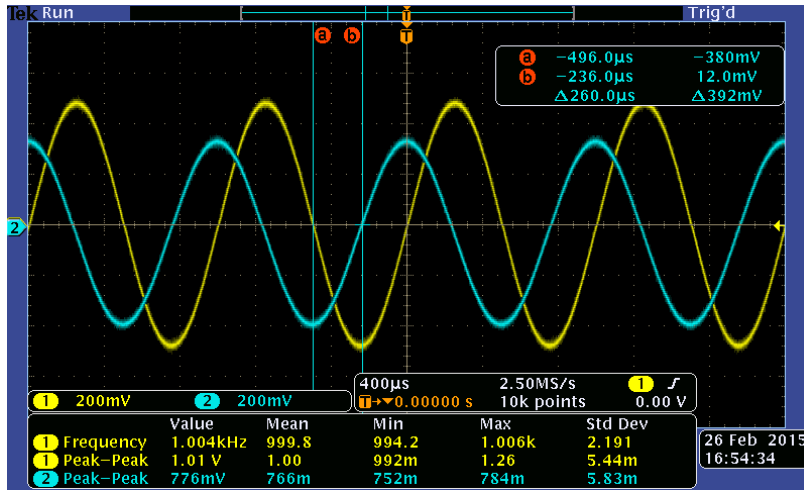
You should have built something like this and gotten results similar to the following for the requested inputs. I found I had to set simulation run time to about .1 s to get it to settle down to a steady state.





4. Build this circuit and capture screenshots with Vin set to be a sine wave, a square wave and a triangle wave = 1.0 Vpp at 1 KHz, 0 V DC offset.

Your results should have been similar to these.



- Reset  $V_{in} = 0.5 V_{pp}$  sine wave at 1 KHz, 0 V DC offset. While it's running, watch the oscilloscope as you remove R2 and then put it back. Describe what you observed. What is the purpose of R2?

$V_{out}$  quickly dives either toward VCC or VEE. This happens because  $\int_0^t a dt = at$ ; any tiny DC offset will eventually integrate over time into an arbitrarily large value, limited only by the power supply. The purpose of R2 is to bleed that off faster than it accumulates.

## 7 Simple differentiator

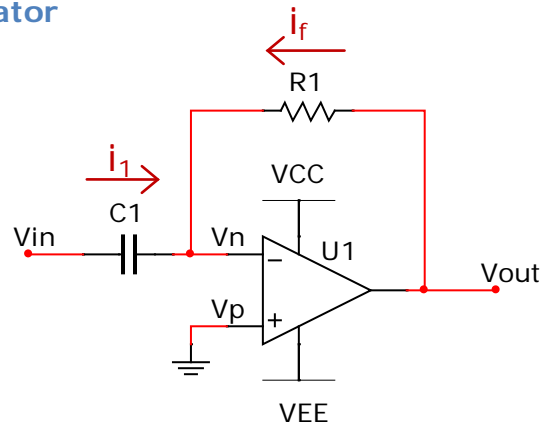


Figure 15. Simple differentiator.

- Analyze the differentiator circuit in figure 15 (same as figure 3) to derive an equation for  $V_{out}(t)$  as a function of  $V_{in}(t)$ . Show that the output is the derivative of the input.

$$V_{out} = i_f R_1$$

$$i_f = \frac{V_{out}}{R_1} = -i_1$$

$$V_{in} = \int_0^t \frac{i_1}{C_1} dt$$

$$V_{in} C_1 = \int_0^t i_1 dt$$

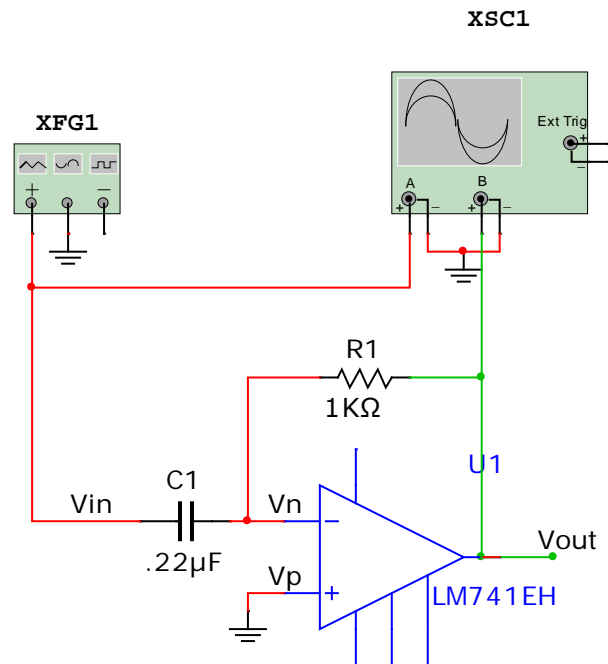
$$i_1 = C_1 \frac{dV_{in}}{dt}$$

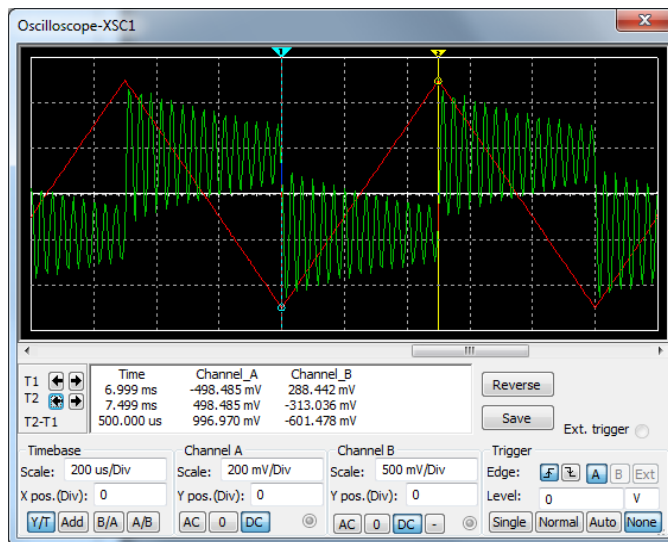
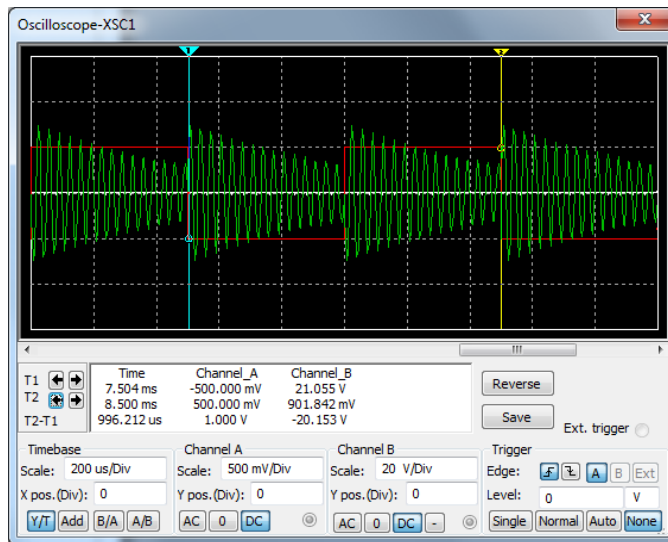
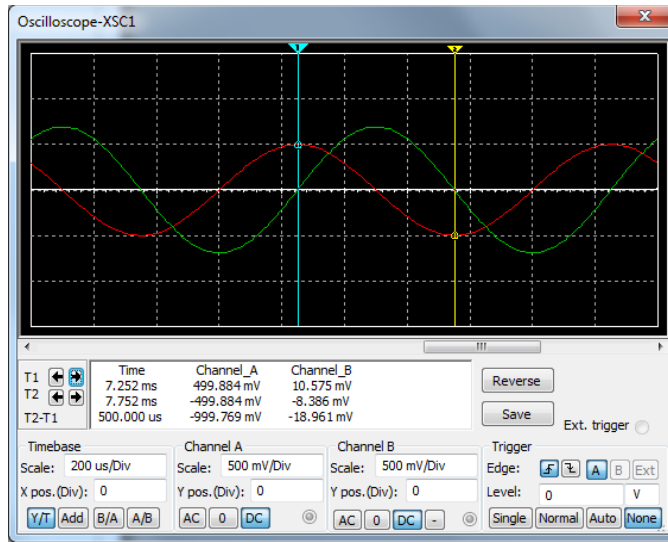
$$i_1 = C_1 \frac{dV_{in}}{dt} = -\frac{V_{out}}{R_1}$$

$$V_{out} = -R_1 C_1 \frac{dV_{in}}{dt}$$

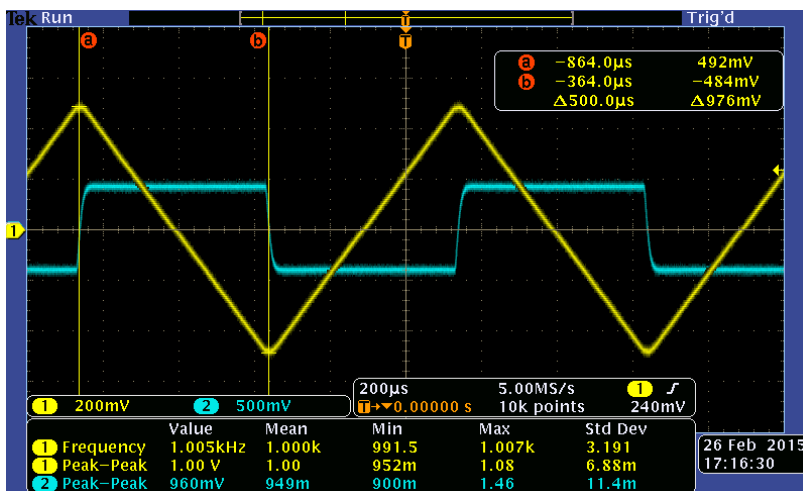
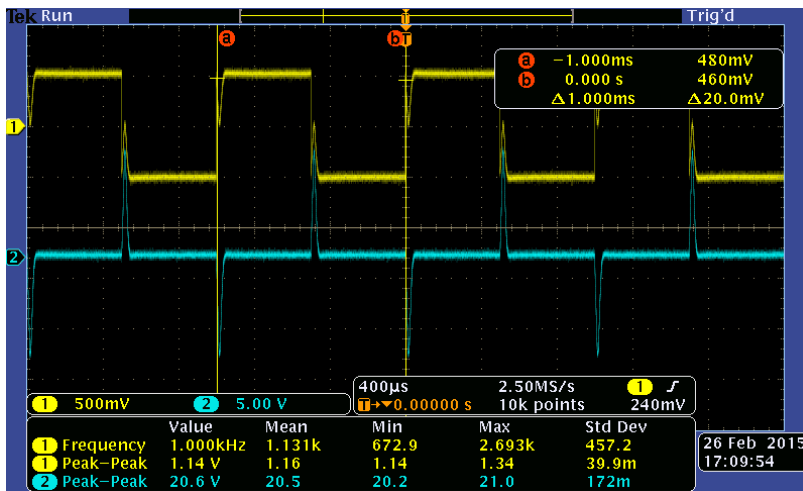
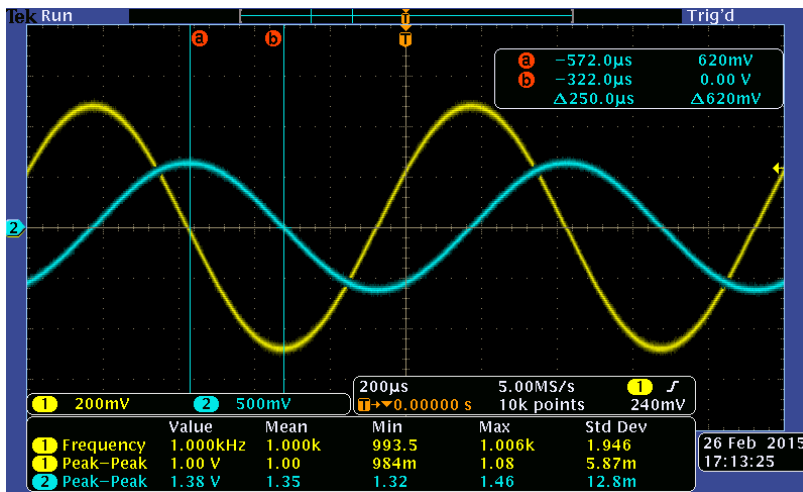
2. Simulate this circuit with  $R_1 = 1 \text{ K}\Omega$  and  $C_1 = 0.22 \text{ }\mu\text{F}$  and capture images of your schematic and of oscilloscope displays of  $V_{in}$  and  $V_{out}$  with  $V_{in}$  set to be a sine wave, a square wave and a triangle wave. In each case, set  $V_{in} = 1.0 \text{ Vpp}$  at  $1 \text{ KHz}$ ,  $0 \text{ V DC}$  offset.

You should have built something like this and may have gotten results similar to the following, predicting that the circuit will work for sine wave input but exhibit severe "ringing" (oscillating) for square and triangle wave inputs.





3. Build this circuit with  $R1 = 1\text{ K}\Omega$  and  $C1 = 0.22\ \mu\text{F}$  and capture screenshots with  $V_{in}$  set to be a sine wave, a square wave and a triangle wave =  $1.0\text{ V}_{pp}$  at  $1\text{ KHz}$ ,  $0\text{ V DC}$  offset.



- Describe what you observe. Does the circuit work as you expected? Can you explain the behavior?

The real circuit works, behaving the way the math predicts and does not exhibit the ringing predicted by the model. The only noticeable artifact is the blip on  $V_{in}$  when the input is a square wave, caused by the output pulse feeding back through  $C1$ . Apparently, the Multisim model is wrong. (Surprise. It's software.)

## 8 Low pass filter

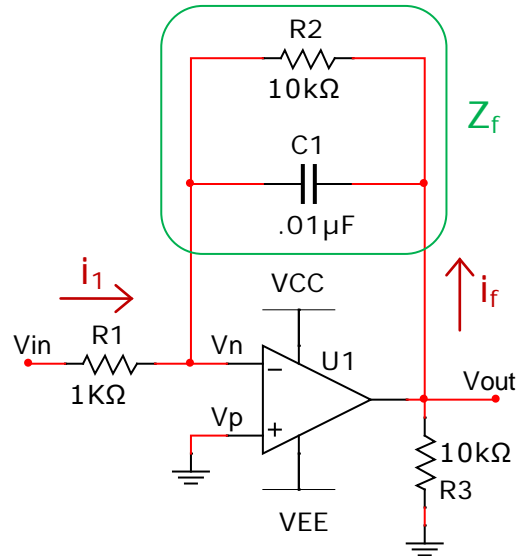


Figure 16. Low-pass filter.

- Analyze the low-pass filter circuit in figure 16 (same as figure 5) to show that for  $V_{in}(t) = A\cos(\omega t)$ :

$$V_{out}(t) = -\frac{R_2}{R_1} A \cos(\omega t) \left( \frac{1 - j\omega R_2 C_1}{1 + \omega^2 R_2^2 C_1^2} \right)$$

$$Y_f = \frac{1}{R_2} + sC_1$$

$$Z_f = \frac{1}{Y_f} = \frac{1}{\frac{1}{R_2} + sC_1} = \frac{R_2}{1 + sR_2C_1}$$

$$i_f = \frac{V_{out}}{Z_f} = V_{out} \left( \frac{1 + sR_2C_1}{R_2} \right)$$



$$i_1 = \frac{V_{in}}{R_1}$$

$$i_f = -i_1$$

$$\frac{V_{in}}{R_1} = -V_{out} \left( \frac{1 + sR_2C_1}{R_2} \right)$$

$$\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1} \left( \frac{1}{1 + sR_2C_1} \right)$$

$$V_{in} = A \cos(\omega t)$$

$$s = j\omega$$

$$\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1} \left( \frac{1}{1 + j\omega R_2 C_1} \right)$$

$$\left( \frac{1}{1 + j\omega R_2 C_1} \right) \left( \frac{1 - j\omega R_2 C_1}{1 - j\omega R_2 C_1} \right) = \left( \frac{1 - j\omega R_2 C_1}{1 + R_2^2 C_1^2} \right)$$

$$\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1} \left( \frac{1 - j\omega R_2 C_1}{1 + \omega^2 R_2^2 C_1^2} \right)$$

$$V_{out} = -\frac{R_2}{R_1} \left( \frac{1 - j\omega R_2 C_1}{1 + \omega^2 R_2^2 C_1^2} \right) V_{in}$$

$$V_{out} = -\frac{R_2}{R_1} A \cos(\omega t) \left( \frac{1 - j\omega R_2 C_1}{1 + \omega^2 R_2^2 C_1^2} \right)$$

2. Show that for the component values shown, the voltage gain,  $A_v$ , of this circuit is:

$$A_v = \frac{V_{out}}{V_{in}} = -\frac{10^5}{\sqrt{10^8 + \omega^2}}$$

$$A_v = \frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1} \left( \frac{1}{1 + j\omega R_2 C_1} \right)$$

$$R_1 = 1K = 10^3$$

$$R_2 = R_3 = 10K = 10^4$$

$$C_1 = 0.01 \mu F = 10^{-8}$$

$$Av = -\frac{10^4}{10^3} \left( \frac{1}{1 + j\omega(10^4)(10^{-8})} \right) = -10 \left( \frac{1}{1 + j\omega(10^{-4})} \right)$$

To get from here to the requested form, you have to notice that  $j\omega(10^{-4})$  will be small compared to 1 since this is intended as a low-pass filter, allowing us to approximate with the magnitude of that complex denominator. (I probably should have rewritten this question to ask for  $|Av|$ , not  $Av$ , and will next time.) Notice that when  $\omega$  is very small,  $Av = -10$  as expected.

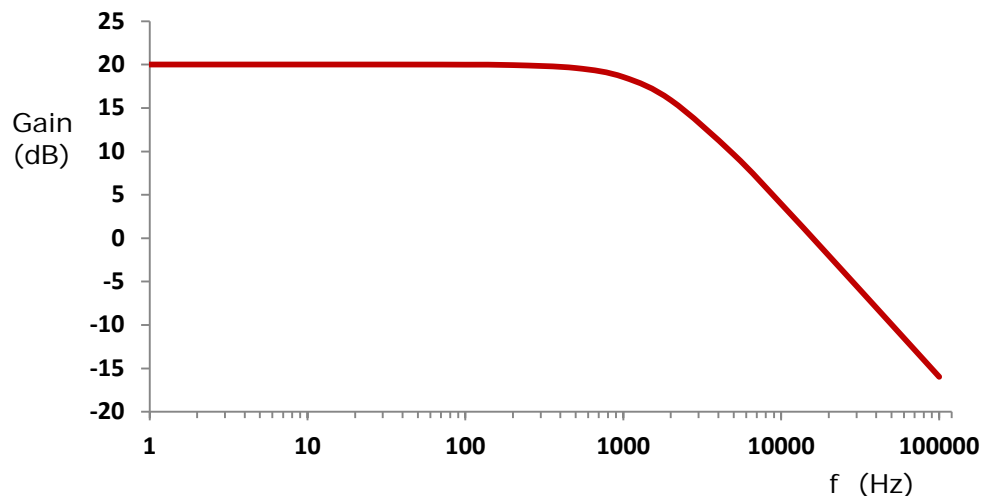
$$|1 + j\omega(10^{-4})| = \sqrt{1 + \omega^2(10^{-8})}$$

$$Av \cong -10 \left( \frac{1}{\sqrt{1 + \omega^2(10^{-8})}} \right)$$

To get it into the final requested form, multiply top and bottom by  $10^4$ .

$$Av = -10 \left( \frac{1}{\sqrt{1 + \omega^2(10^{-8})}} \right) \left( \frac{10^4}{10^4} \right) = -\frac{10^5}{\sqrt{10^8 + \omega^2}}$$

3. Create a Bode plot of the expected gain from 1 Hz to 100 KHz and calculate the expected cutoff frequency.



Gain at low frequency is 20 dB =  $20 \log_{10}(|Av|) = 20 \log_{10}(10)$ . The cutoff frequency is the point at which gain has dropped by 3 dB to 17 dB.

$$17 = 20 \log_{10}(|Av|)$$

$$\frac{17}{20} = \log_{10}(|Av|)$$

$$10^{\frac{17}{20}} = |Av| = 7.079$$

$$\frac{10^5}{\sqrt{10^8 + \omega^2}} = 7.079$$

$$\frac{10^5}{7.079} = \sqrt{10^8 + \omega^2} = 14125.37$$

$$10^8 + \omega^2 = 14125.37^2 = 199526231.5$$

$$\omega^2 = 199526231.5 - 10^8 = 99526231.5$$

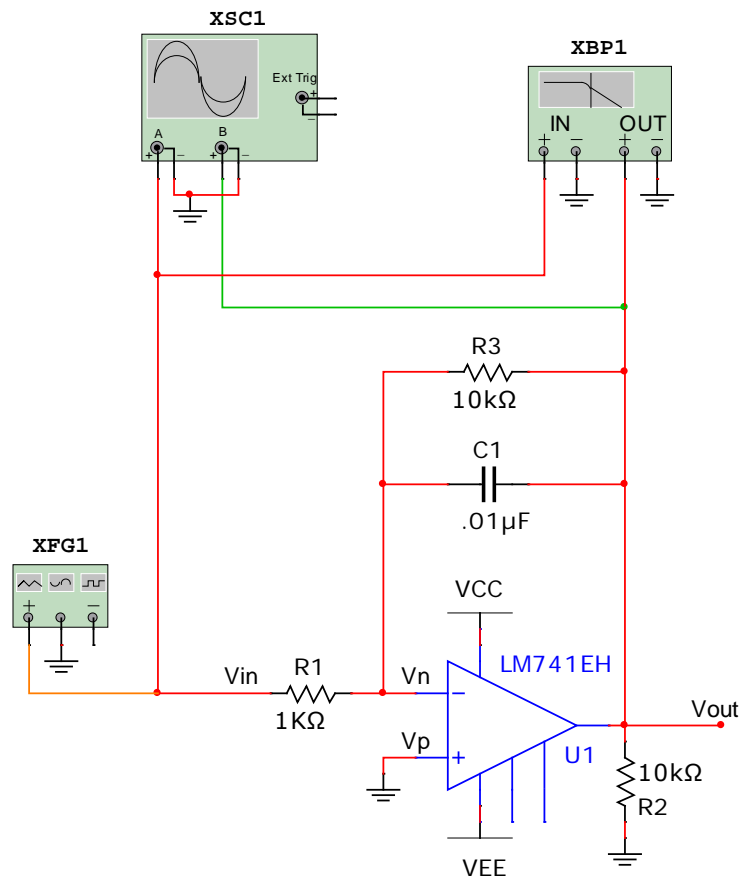
$$\omega = 9976.28 \text{ radians/s}$$

$$f = \frac{\omega}{2\pi} = 1587.77 \text{ Hz}$$

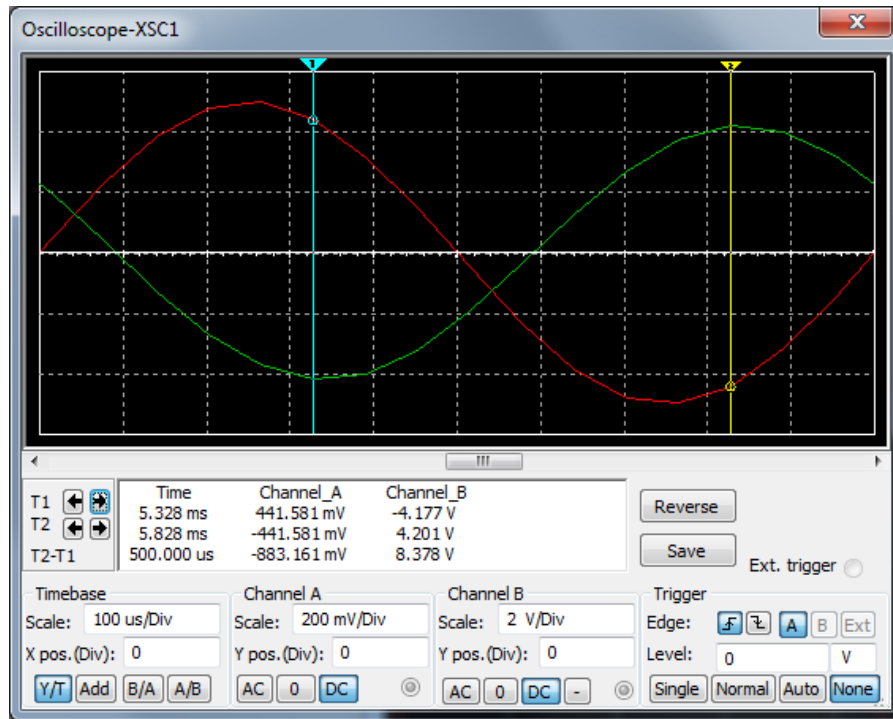
4. Simulate your circuit. Capture images of the following.

a. Your schematic.

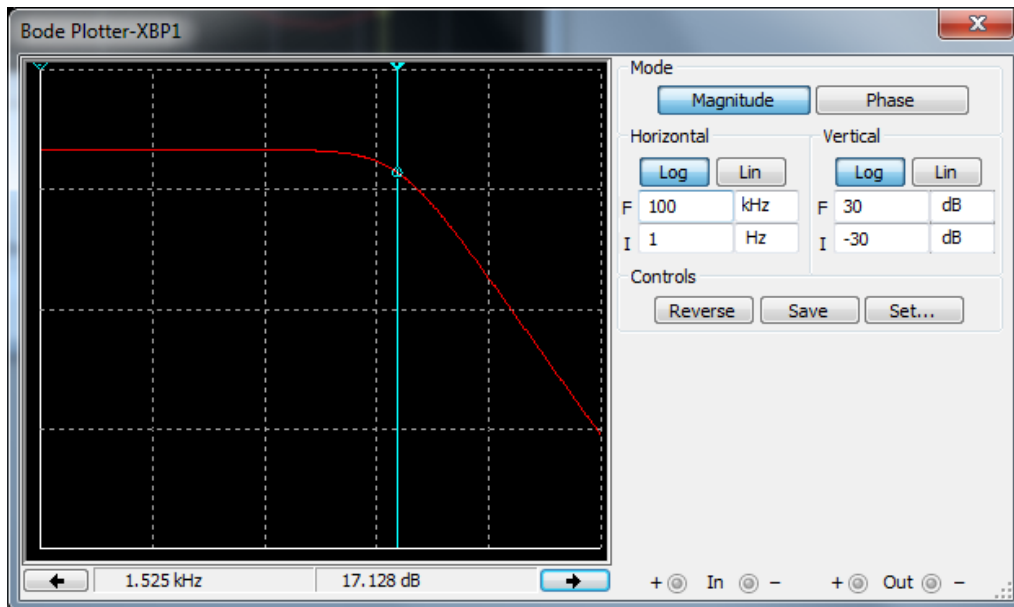
You should have built something like this and gotten similar results.



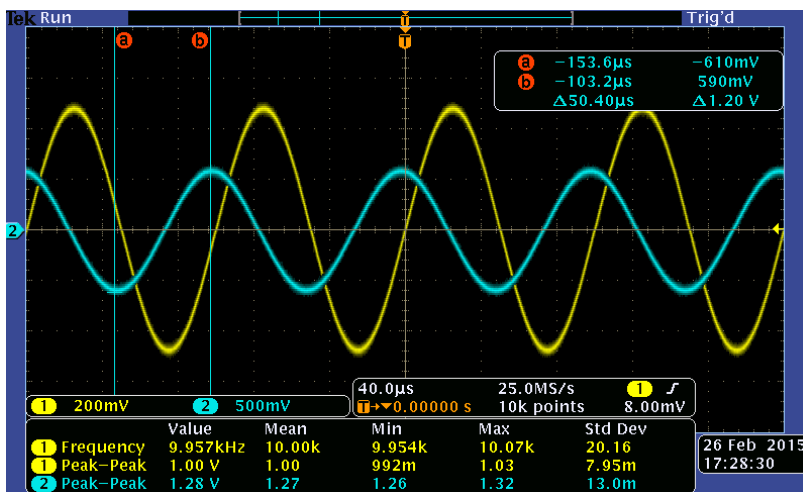
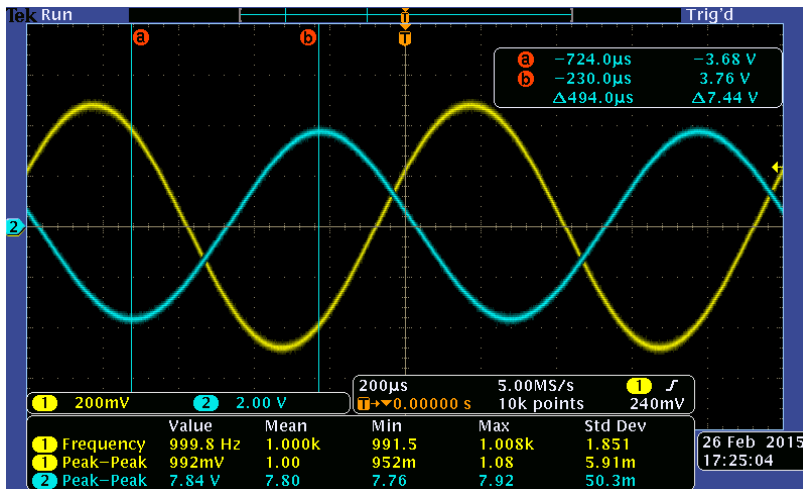
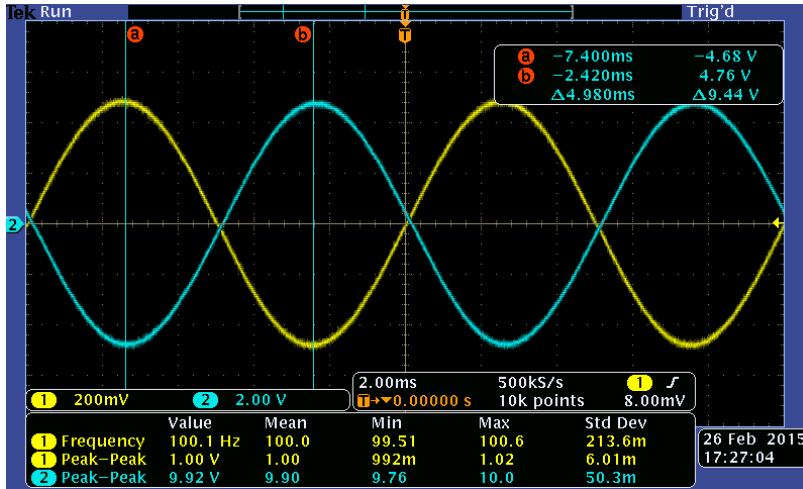
- b. An oscilloscope display of  $V_{in}$  and  $V_{out}$  for  $V_{in} = 1.0$  Vpp, 1 KHz sine wave, 0 V DC offset.



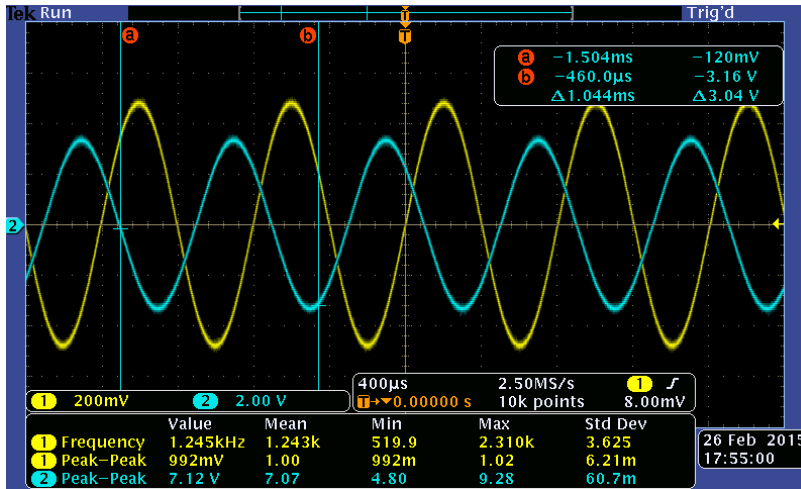
- c. A Bode plot of the frequency response with a cursor at the 3 dB point.



5. Breadboard the circuit and capture screenshots with  $V_{in} = 1.0$  Vpp sine wave, 0 V DC offset, at 100 Hz, 1 KHz and 10 KHz.



6. Find the frequency at which gain has dropped by 3 dB and capture a screenshot.



7. Create a table of measurements at increasing frequencies from 100 Hz to 100 KHz in a 1-2-5-10 sequence. Try to hold  $V_{in}$  fairly constant as you increase the frequency.

Frequency (Hz)	$V_{in}$	$V_{out}$	Gain ( $A_v$ )	Gain (dB)
100	Your data goes here			
200				
500				
1K				
2K				
:				
50K				
100K				

8. Create a Bode plot of Gain(dB) versus frequency from your measurements.

Your plot goes here.

9. Compare your three Bode plots and cutoff frequencies based on your calculations, your simulation and your experimental results and explain any differences.

Your calculated and simulated results should have agreed pretty well but it wouldn't be surprising if your measured values are off due to component tolerances. Here were my results.

	Cutoff frequency (Hz)
Calculated	1588
Simulated	1525
Measured	1245